

ABSTRACT

A microprocessor chip, and methods for use in that microprocessor chip. The chip has instruction pipeline circuitry and address translation circuitry. Table lookup circuitry indexes into a table, the table having an entry associated with each corresponding address range translated by the address translation circuitry. Each entry of the table describes a likelihood of the existence of an alternate coding of instructions located in the respective corresponding address range. The table lookup circuitry retrieves a table entry corresponding to the address, and is operable as part of the basic instruction cycle of executing an instruction of a non-supervisor mode program executing on a computer. Interrupt circuitry is cooperatively designed with the instruction pipeline circuitry to trigger an interrupt on execution of an instruction of a process, synchronously based at least in part on a memory state of the computer and the address of the instruction, the architectural definition of the instruction not calling for an interrupt. A handler for the interrupt is responsive to the contents of the table to affect the instruction pipeline circuitry to effect control of an architecturally-visible data manipulation behavior or control transfer behavior of the instruction based on the contents of a table entry associated with the instruction.

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